What is claimed is:

1. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnect to the first, second and third conductor layers.

2. The multi layer integrated circuit capacitor of claim 1 further comprising a plurality of controlled collapse chip connection (C4) lands fabricated on the third insulator layer and in electrical contact with the plurality of conductive vias.

3. The multi layer integrated circuit capacitor of claim 2 wherein the C4 lands are fabricated in staggered columns in a plan view.

4. The multi layer integrated circuit capacitor of claim 1 wherein the conductor layers comprise a metal material and the insulator layers comprise $BaSrTiO_3$.

5. The multi layer integrated circuit capacitor of claim 4 wherein the conductor layers are fabricated from a copper.

6. The multi layer integrated circuit capacitor of claim 1 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

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7. The multi layer integrated circuit capacitor of claim 1 wherein the second and third conductive layers are fabricated in a plurality of strips, such that a surface area of the second conductive layer is less than a surface area of the first conductive layer and a surface area of the third conductive layer is less than the surface area of the second conductive layer.

8. The multi layer integrated circuit capacitor of claim 1 wherein some of the plurality of conductive vias pass through the second conductive layer without forming an electrical connection with the second conductive layer.

9. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer, the second conductive layer is fabricated as a plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer, the third conductive layer is fabricated as a plurality of laterally spaced strips such that a surface area of the third conductive layer is less than the surface area of the second conductive layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnect to the third conductive layer;

a second plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnect to the second conductive layer; and

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a third plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnect to the first conductive layer.

10. The multi layer integrated circuit capacitor of claim 9 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

11. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer, third conductive layer, second insulator layer, second conductive layer and the first insulator layer to provide electrical interconnect to the first and third conductive layers; and

a second plurality of conductive vias downwardly extending through the third insulator layer, third conductive layer and second insulator layer to provide electrical interconnect to the second conductive layer.

12. The multi layer integrated circuit capacitor of claim 11 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

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13. The multi layer integrated circuit capacitor of claim 11 wherein the conductive layers comprise a metal material and the insulator layers comprise $BaSrTiO_3$.

14. A circuit package comprising:

a package having a pair of supply voltage interconnect lines;

a first integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines; and

a second integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines, the second integrated circuit package comprises a capacitor having:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnect to the first, second and third conductive layers.

15. The circuit board assembly of claim 14 wherein the second integrated circuit package comprises a plurality of controlled collapse chip connection (C4) lands that are electrically connected to the plurality of conductive vias and the supply voltage interconnect lines.

16. The circuit board assembly of claim 14 wherein the first integrated circuit package is a processor circuit.

17. The circuit board assembly of claim 14 wherein the conductive layers comprise a metal material and the insulator layers comprise $BaSrTiO_3$.

18. The circuit board assembly of claim 14 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

19. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnect to the first, second and third conductive layers, the plurality of conductive vias further extend through the substrate to provide electrical interconnects on both a top and a bottom surface of the integrated circuit capacitor.

20. The multi layer integrated circuit capacitor of claim 19 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

21. The multi layer integrated circuit capacitor of claim 1 wherein the conductor layers comprise a metal material and the insulator layers comprise $BaSrTiO_3$.